REMARKS

Claims 1-16, 41-50, and 66-85 are pending in the application. The Applicants' attorney has amended claims 7-8, 43-44, 71-72, and 84-85. As discussed below, the claims are in condition for allowance. **But if after considering this response the Examiner does not agree that all of the claims are allowable, he is respectfully requested to schedule and conduct a telephone interview with the Applicants' attorney before issuing a subsequent Office Action. The Applicants' attorney left a voice mail for the Examiner on 06 July 2009 to schedule an interview.**

Information Disclosure Statement

The Examiner states that he has not considered the two NPL references cited in the IDS filed on 17 February 2009, because he already cited these two references in a form PTO-892 mailed 13 November 2008. Therefore, the Applicants' attorney understands the Examiner's statement to mean that the Examiner has already considered these two references, and asks the Examiner to confirm this understanding in writing.

Citation Of Wu As Extrinsic Evidence

The Examiner has cited a reference to Wu et al. as extrinsic evidence, but has not based any of his rejections on Wu. Therefore, the Applicants' attorney does not address Wu in his arguments for patentability. If the Examiner intended to reject the claims based on Wu, then he is requested to issue a subsequent non-final Office Action including such a rejection.

The Examiner's Taking Of Official Notice

The Examiner has taken official notice that "hardware and software are logically equivalent and that anything performed by software can be performed solely by hardware and vice versa."

But the Applicants' attorney challenges the Examiner's statement, and requests

documentary support for this statement, because the Applicants' attorney believes that the Examiner's statement is inaccurate. Can a temperature sensor be implemented solely in software? Can the functions performed by Microsoft Windows® be performed solely in hardware? And if the functions performed by Microsoft Windows® can theoretically be performed solely in hardware, can these functions be practically performed solely in hardware with today's technology?

Rejection Of Claims 1-5, 7, 9-10, 12, 15-16, 41-45, 49-50, 69-72, 76-79, And 83-85 Under 35 U.S.C. § 103(a) As Being Unpatentable Over U.S. 2003/014627 To Krishna In View Of U.S. 6,028,939 To Yin, And Further In View Of The Examiner's Taking Of Official Notice

Claim 1

Claim 1 as previously pending recites a hardwired-pipeline circuit operable, without executing a program instruction, to receive a message that includes data and that includes a header having information indicating a destination of the data, to extract the data from the message, to load the extracted data into the memory, to retrieve the extracted data from the memory, and to process the retrieved data with a pipeline corresponding to the destination.

For example, referring, *e.g.*, to FIGS. 4-5 and paragraphs [51], [57], and [97] – [100] of the patent application, in an embodiment, a pipeline circuit 80 (FIG. 4) has an input-data handler 120 (FIG. 5) operable, without executing a programming instruction, to receive via a pipeline bus 50 (see also FIG. 3) a message that includes data and that includes a header having information indicating a destination pipeline 74 for the data by receiving the data and information on at least one common line of the pipeline bus 50, to extract the data from the message, and to load the extracted data into a memory 92. An interface 140 is operable, without executing a program instruction, to retrieve the extracted data from the memory 92, and the destination pipeline 74 is operable, without executing a program instruction, to process the retrieved data.

In contrast, the combination of Krishna, Yin, and the Examiner's taking of Official Notice do not render claim 1 obvious as discussed below.

1) The Examiner has failed to make a prima facie showing of obviousness because Krishna does not disclose processing data received in a message with a pipeline corresponding to a destination included in a header of the message. Referring to Krishna's FIGS. 2 and 3, packets are received into an input FIFO 202/302. Referring to paragraph [0038], the header information for a packet in the FIFO 202/302 is provided to a packet classifier unit 204/304, which determines security association information required for processing the packet. Referring to paragraphs [0039], [0041], [0042], and [0053], a packet distributor 206/306 provides the packet data and the security association information for the packet to one of a plurality of processing engines 214/316 in round-robin order according to stored microcode to improve processing performance. That is, the packet distributor 206/306 does not provide a packet and its security association information to a particular processing engine 214/316 based on a data-destination address stored in the packet header. This analysis of Krishna is confirmed by the table on p. 7, which shows that although a packet header may include IP and TCP addresses, the packet header does not include an address indicating a particular packet distributor 206/306 for processing the packet data.

2) Even if Krisha were to disclose processing data received in a message with a pipeline corresponding to a destination included in a header of the message, the combination of Krishna, Yin, and the Examiner's taking of Official Notice does not render claim 1 obvious.

a) As the Examiner correctly points out, Krishna does not disclose performing the following message-related steps recited in claim 1 without executing a program instruction: receiving a message that includes data and that includes a header having information indicating a destination of the data, extracting the data from the message, loading the extracted data into the memory, retrieving the extracted data from the memory, and processing the retrieved data with a pipeline corresponding to the destination (as stated above, Krishna does not even disclose performing this step in software).

And not only does Yin fail to disclose performing these message-related steps without executing a program instruction, Yin fails to disclose performing these steps in any manner. Referring to FIG. 9 and col. 9, lines 24-60, although Yin discloses a programmable hardware element (PHE) 210 communicating with busses 206 and 216, these busses do not carry messages having headers, but instead carry separate address and data signals. Therefore, because Yin does not disclose transferring data via messages, Yin does not disclose any of the message-related functions disclosed in Krishna or any of the message-related steps recited in claim 1.

The Examiner's reasoning seems to be that because Yin discloses that one may use a PHE to perform Data Encryption Standard (DES) processing, that it would be obvious that one could use a PHE to perform *any* software function, such as the message-related functions disclosed in Krishna.

But the Examiner's reasoning is flawed. Yin actually teaches away from performing *any* software function in hardware, because Yin teaches that it is better to perform some functions in hardware and other functions in software (col. 3, lines 18-20, col. 7, lies 20-28, col. 9 lines 40-59, col. 10 lines 22-39, and col. 11 lines 13-19), and even states that a same function may be best performed in hardware sometimes and in software other times depending on the function parameters (col. 12, lines 45-65). Furthermore, as stated above, Yin fails to even mention the message-related functions recited in Krishna. And Yin fails to provide any indication as to whether it is best to perform the message-related functions of Krishna in hardware or in software. Therefore, there is no way that one can glean from Yin a suggestion or motivation to perform the message-related functions of Krisha in a PHE.

b) Irrespective of whether the Examiner's statement (challenged above) of which he takes official notice proves to be accurate, the question under 35 U.S.C. § 103(a) is not whether something is possible, but is instead whether something is obvious.

Consequently, even if the Examiner's statement that anything performed in software can be performed solely in hardware proves to be accurate, claim 1 is still

not rendered obvious by the combination of Krishna and the Examiner's statement of official notice, because even the Examiner's own reference, Yin, teaches that even though some functions may be performed in hardware, these functions are best performed in software. That is, just because a function can theoretically be performed in either software or hardware does not mean that it is an obvious design choice to perform the function in hardware.

For the reasons set forth above, the Examiner has failed to show that claim 1 is obvious, and, therefore, he must withdraw this rejection of claim 1.

Claims 2-5

These claims are patentable by virtue of their respective dependencies from claim 1.

Claim 7

Claim 7 as amended recites a hardwired-pipeline circuit operable, without executing a program instruction, to receive data without receiving with the data information corresponding to a post-processing destination of the data, to process the received data, and to generate a message header that includes information indicating a destination of the processed data.

For example, referring, *e.g.*, to FIGS. 4-5 and paragraphs [51], [57], [82] – [84], and [100] – [104] of the patent application, in an embodiment, a pipeline circuit 80 (FIG. 4) includes at least one pipeline 74 (FIG. 5) that is operable, without executing a program instruction, to receive data from a DPSRAM 100 without receiving post-processing-destination information corresponding to this data, and to process the received data. An output-data handler 126 (FIG. 5) is operable, without executing a program instruction, to generate a message header that includes information indicating a destination of the processed data.

In contrast, the combination of Krishna, Yin, and the Examiner's official notice fails to disclose or suggest a hardwired-pipeline circuit operable to receive data without receiving

with the data information corresponding to a post-processing destination of the data, and to generate a message header that includes information indicating a destination of the processed data.

Referring to Krishna's p. 7 and FIG. 3, the input FIFO 302 receives a packet that includes a header having an IP and/or TCP destination address. This header is parsed, processed, and then reassembled with the data into a packet that is stored in the output FIFO 318 for transmission. Therefore, unlike the hardwired-pipeline circuit recited in claim 7, Krishna's chip 300 receives data and also receives information corresponding to a post-processing destination of the data.

Furthermore, as discussed above, Yin does not discuss whether the PHE 210 (FIG. 9) receives with data information corresponding to a post-processing destination of the data, and does not discuss message headers.

And, even if the Examiner's statement of which he takes official notice is accurate, the Examiner's statement does not encompass data destinations or message headers.

Claim 9

Claim 9 as previously pending recites an input-data handler operable without executing a program instruction to receive a message that includes raw data and a header having information indicating a destination of the raw data, and a pipeline interface operable without executing a program instruction to provide the retrieved raw data to a hardwired pipeline corresponding to the destination.

Therefore, although the scope of claims 1 and 9 may not be the same, claim 9 is patentable for reasons similar to those recited above in support of the patentability of claim 1.

Claims 10, 12, and 15-16

These claims are patentable by virtue of their dependencies from claim 9.

Claims 41, 44, 76, and 78-79

Although the scopes of these claims may not be the same, and may be different from the scopes of claims 1 and 9, these claims are patentable for reasons similar to those recited above in support of the patentability of claims 1 and/or 9.

Claims 43, 71-72, and 84-85

Although the scopes of these claims may not be the same, and may be different from the scope of claim 7, these claims are patentable for reasons similar to those recited above in support of the patentability of claim 7.

Claims 10, 12, 15-16, 42, 45, 49-50, 69-70, 77, and 83

These claims are patentable by virtue of their dependencies on their respective independent claims.

Rejection Of Claims 6 And 8 Under 35 U.S.C. § 103(a) As Being Unpatentable Over Krishna In View Of Yin, And Further In View Of U.S. 2003/0231649 To Awoseyi And The Examiner's Taking Of Official Notice

Claim 6

Claim 6 as previously pending recites a processor operable to broadcast a message that includes data and that includes a header having information indicating a destination of the data, and a hardwired-pipeline circuit operable, without executing a program instruction, to process the data with a pipeline corresponding to the destination.

For reasons similar to those discussed above in support of the patentability of claim 1, the combination of Krishna, Yin, and the Examiner's statement of which he takes official notice does not render claim 6 obvious.

Furthermore, Awoseyi does not disclose or suggest processing data with a pipeline corresponding to a destination that is indicated in a header of a message that includes the

data.

Consequently, because Awoseyi does not provide the teaching missing from Krishna, Yin, and the Examiner's statement of which he takes official notice, the combination of Krishna, Yin, Examiner's statement, and Awoseyi does not render claim 6 obvious.

Claim 8

Claim 8 as amended recites receiving data from a processor without receiving with the data information corresponding to a post-processing destination of the data, processing the received data, and generating a message header that includes, for the processed data, information that indicates a destination software application running on the processor.

For reasons similar to those discussed above in support of the patentability of claim 1, the combination of Krishna, Yin, and the Examiner's statement of which he takes official notice does not render claim 8 obvious.

Furthermore, Awoseyi does not disclose or suggest receiving data from a processor without receiving with the data information corresponding to a post-processing destination of the data, processing the received data, and generating a message header that includes, for the processed data, information that indicates a destination software application running on the processor.

Consequently, because Awoseyi does not provide the teaching missing from Krishna, Yin, and the Examiner's statement of which he takes official notice, the combination of Krishna, Yin, the Examiner's statement, and Awoseyi does not render claim 8 obvious.

Rejection Of Claims 11 And 46 Under 35 U.S.C. § 103(a) As Being Unpatentable Over Krishna In View Of Yin, And Further In View Of U.S. 2002/0041685 To McLoone

These claims are patentable by virtue of their respective dependencies from claims 9 and 44.

Rejection Of Claims 13, 47, 68, 75, And 82 Under 35 U.S.C. § 103(a) As Being Unpatentable Over Krishna In View Of Yin In View Of Official Notice And Further In View Of U.S. 5,185,871 To Frey

Claim 13

This claim is patentable by virtue of its dependency from claim 9.

Claim 47

This claim is patentable by virtue of its dependency from claim 44.

Claim 68

Claim 68 as previously pending recites a hardwired-pipeline circuit operable, without executing a program instruction, to receive a message that includes data and that includes a header having information indicating a destination of the data, and to process the data with a pipeline corresponding to the destination.

For reasons similar to those discussed above in support of the patentability of claim 1, the combination of Krishna, Yin, and the Examiner's statement of which he takes official notice does not render claim 68 obvious.

Furthermore, Frey does not disclose or suggest processing data with a pipeline corresponding to a destination that is indicated in a header of a message that includes the data.

Consequently, because Frey does not provide the teaching missing from Krishna, Yin, and the Examiner's statement of which he takes official notice, the combination of Krishna, Yin, the Examiner's statement, and Frey does not render claim 68 obvious.

Claims 75 And 82

Although the scopes of these claims may not be the same, and may be different from the scope of claim 68, these claims are patentable for reasons similar to those recited above in support of the patentability of claim 68.

Allowable Subject Matter

Claims 14, 48, 66-67, 73-74, and 80-81 are allowed.

CONCLUSION

In view of the foregoing, in addition to allowed claims 14, 48, 66-67, 73-74, and 80-81, claims 7-8, 43-44, 71-72, and 84-85 as amended, and claims 1-6, 9-16, 41-42, 45-50, 66-70, and 73-83 as previously pending are in condition for allowance. Therefore, the issuance of a formal Notice of Allowance at an early date is respectfully requested.

In the event additional fees are due as a result of this amendment, you are hereby authorized to charge such payment to Deposit Account No. 07-1897.

DATED this 9th day of July, 2009.

Respectfully submitted,

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